AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A memory system comprising:

a memory controller;

at least one memory storage device connected to a memory bus;

a continuous optical path coupled to said memory controller and to said memory bus arranged and configured for exchanging data between said memory controller and said at least one memory storage device, said optical path comprising a first wavelength-adjustable electro-optical converter arranged and configured to convert an electrical signal output from said controller to an optical signal for transmission on said continuous optical path, said memory controller, memory bus and continuous optical path being formed on a single die; and

a wavelength sensing mechanism connected to said controller arranged and configured to provide wavelength information to said controller with respect to an optical signal on said continuous optical path.

2. (Previously Presented) The memory system of claim 1, wherein said memory controller and said at least one memory storage device are arranged and configured to exchange data exclusively through said optical path.

3. (Previously Presented) The memory system of claim 1, wherein said controller and said at least one memory storage device are arranged and configured to exchange read/write data through said optical path.

4. (Previously Presented) The memory system of claim 1, wherein said continuous optical path includes at least one optical link for exchange of read/write data.

5. (Previously Presented) The memory system of claim 1, wherein said continuous optical path includes at least one optical link for address data transmitted from said memory controller to said at least one memory storage device.

6. (Previously Presented) The memory system of claim 1, wherein said continuous optical path includes an optical link for command data transmitted from said memory controller to said at least one memory storage device.

7. (Previously Presented) The memory system of claim 1, wherein said continuous optical path includes an optical link for transmission of a clock signal to the at least one memory storage device.

8. (Previously Presented) The memory system of claim 1, wherein said continuous optical path includes an optical link for transmission of control data to the at least one memory storage device.

9. (Previously Presented) The memory system of claim 1, wherein said continuous optical path comprises a plurality of multiplexed optical channels.

10-11. (Canceled)

12. (Previously Presented) The memory system of claim 1, further comprising a second electro-optical converter arranged and configured to convert an optical signal transmitted on said optical path to an electrical signal and to transmit said electrical signal to said memory controller.

13. (Canceled)

14. (Previously Presented) The memory system of claim 1 further comprising:

a second electro-optical converter arranged and configured to convert an optical signal on said continuous optical path to an electrical signal and for transmitting said electrical signal to said at least one memory storage device.

15. (Previously Presented) The memory system of claim 9, further comprising:

a multiplexer optically connected with said controller arranged and configured for multiplexing said optical channels, and

a demultiplexer optically connected with said at least one memory storage device arranged and configured for demultiplexing said multiplexed optical channels.

16. (Previously Presented) The memory system of claim 9, further comprising:

a multiplexer optically connected with said at least one memory storage device arranged and configured for multiplexing optical channels and providing multiplexed optical channels to said continuous optical path; and

a demultiplexer optically connected with said memory controller arranged and configured for demultiplexing said multiplexed optical channels.

17. (Previously Presented) The memory system of claim 9, further comprising:

a respective optical multiplexer and demultiplexer on each end of said continuous optical path.

18. (Previously Presented) The memory system of claim 17, wherein said respective optical multiplexer and demultiplexer are arranged and configured to convert signal data that includes at least read/write data.

19. (Previously Presented) The memory system of claim 17, wherein said signal data includes command data.

20. (Previously Presented) The memory system of claim 17, wherein said signal data includes address data.

21. (Previously Presented) The memory system of claim 17, said signal data includes a clock signal.

22. (Previously Presented) The memory system of claim 17, wherein said signal data includes control data.

23. (Previously Presented) The memory system of claim 17, further comprising:

electrical data paths connected between said memory controller and said at least one memory storage device.

24. (Previously Presented) The memory system of claim 1, wherein said at least one memory storage device is located on a memory module.

25. (Previously Presented) The memory system of claim 24, further comprising:

an optical coupler disposed at said memory module arranged and configured to connect said memory storage device to said continuous optical path.

26. (Canceled)

27. (Previously Presented) The memory system of claim 1, wherein said wavelength sensing mechanism is located at a controller side of said continuous optical path.

28. (Previously Presented) The memory system of claim 1, wherein said controller is arranged and configured to provide wavelength adjustment information to said first wavelength-adjustable converter.

29. (Previously Presented) The memory system of claim 1, wherein said continuous optical path comprises a single optical path between said controller and at least one memory storage device arranged and configured for exchanging at least read/write data between said controller and at least one memory storage device.

30. (Previously Presented) The memory system of claim 29 wherein said single optical path further is arranged and configured to exchange command data between said memory controller and at least one memory storage device.

31. (Previously Presented) The memory system of claim 29 wherein said single optical path further is arranged and configured to exchange address data between said memory controller and at least one memory storage device.

32. (Previously Presented) The memory system of claim 29 wherein said single optical path further is arranged and configured to pass a clock signal between said memory controller and at least one memory storage device.

33. (Previously Presented) The memory system of claim 1 wherein said data includes read/write data which originates on a plurality of electrical paths, said continuous optical path comprising a plurality of discrete optical guides respectively associated with said plurality of electrical paths.

34. (Previously Presented) The memory system of claim 1 wherein said data includes command data which originates on a plurality of electrical paths, said continuous optical path comprising a plurality of discrete optical guides respectively associated with said plurality of electrical paths.

35. (Previously Presented) The memory system of claim 1 wherein said data includes address data which originates on a plurality of electrical paths, said continuous optical path comprising a plurality of discrete optical guides respectively associated with said plurality of electrical paths.

36. (Previously Presented) The memory system of claim 1 wherein said data includes clock signal data which originates on an electrical path, said continuous optical path comprising a discrete optical guide respectively associated with said electrical path.

37. (Canceled)

38. (Previously Presented) The memory system of claim 1 wherein said data includes control signal data which originates on an electrical signal path, said continuous optical path comprising a discrete optical guide associated with said electrical signal path.

39. (Canceled)

40. (Previously Presented) The memory system of claim 1, further comprising:

a processor, for communicating with said at least one memory storage device, wherein said controller, at least one memory storage device, processor, and continuous optical path are all integrated on the same die.

41-43. (Canceled)

44. (Previously Presented) The memory system of claim 24, wherein said memory module comprises an electro-optical converter arranged and configured for connecting optical data from said continuous optical path to electrical signals for said at least one memory storage device.

45. (Previously Presented) A computer system, comprising:

a processor; and

a memory system connected to said processor, said memory system comprising:

a memory controller;

at least one memory storage device;

an optical path coupled at a first end to said memory controller and at a second end to a bus connecting with said at least one memory storage device for optically exchanging data between said memory controller and said at least one memory storage device, said optical path comprising a first wavelength-adjustable electro-optical converter arranged and configured to convert an electrical signal output from said memory controller to an optical signal for transmission on said optical path, said memory controller, bus and continuous optical path being formed on a single die; and

a wavelength sensing mechanism connected to said memory controller, for providing wavelength information to said memory controller with respect to an optical signal on said optical path.

46. (Previously Presented) A computer system of claim 45, wherein said memory controller and said at least one memory storage device are arranged and configured to exchange data exclusively through said optical path.

47. (Previously Presented) A computer system of claim 45, wherein said memory controller and said at least one memory storage device are arranged and configured to exchange read/write data through said optical path.

48. (Previously Presented) A computer system of claim 45, wherein said optical path includes at least one optical link for exchange of read/write data.

49. (Previously Presented) A computer system of claim 45, wherein said optical path includes an optical link for address data transmitted from said memory controller to said at least one memory storage device.

50. (Previously Presented) A computer system of claim 45, wherein said optical path includes an optical link for command data transmitted from said memory controller to said at least one memory storage device.

51. (Previously Presented) A computer system of claim 45, wherein said optical path includes an optical link for transmission of a clock signal to the at least one memory storage device.

52. (Previously Presented) A computer system of claim 45, wherein said optical path includes an optical link for transmission of control data to the at least one memory storage device.

53. (Previously Presented) A computer system of claim 45, wherein said optical path comprises a plurality of multiplexed optical channels.

54-55. (Canceled)

56. (Previously Presented) A computer system of claim 45, further comprising a second electro-optical converter arranged and configured to convert an optical signal transmitted on said optical path to an electrical signal.

57. (Canceled)

58. (Previously Presented) A computer system of claim 45, comprising a second electro-optical converter for converting an optical signal on said optical path to an electrical signal an transmitting said electrical signal to said at least one memory storage device.

59. (Previously Presented) A computer system of claim 52, comprising a multiplexer associated with said memory controller for multiplexing said optical channels, and

a demultiplexer associated with said at least one memory storage device for demultiplexing said multiplexed optical channels.

60. (Previously Presented) A computer system of claim 52, comprising a multiplexer associated with said at least one memory storage device for multiplexing optical channels and providing multiplexed optical channels to said optical path; and

a demultiplexer associated with said memory controller for demultiplexing said multiplexed optical channels.

61. (Original) A computer system of claim 52, comprising an optical multiplexer and demultiplexer located on each side of said optical path.

62. (Previously Presented) A computer system of claim 61, wherein said data includes at least read/write data.

63. (Original) A computer system of claim 61, wherein said data includes command data.

64. (Previously Presented) A computer system of claim 61, wherein said data includes address data.

65. (Original) A computer system of claim 61, wherein said data includes a clock signal.

66. (Original) A computer system of claim 61, wherein said data includes control data.

67. (Previously Presented) A computer system of claim 61, further comprising:

electrical paths connected between said memory controller and said at least one memory storage device for passing data between said controller and said at least one memory storage device.

68. (Previously Presented) A computer system of claim 45, wherein said at least one memory storage device is located on a memory module.

69. (Original) A computer system of claim 68, further comprising:

an optical coupler at said memory module, having a connector for connecting with said optical path.

70. (Canceled)

71. (Previously Presented) A computer system of claim 45, wherein said wavelength sensing mechanism is located at a controller side of said optical path.

72. (Previously Presented) A computer system of claim 45, wherein said memory controller provides wavelength adjustment information to said first wavelength-adjustable converter.

73. (Previously Presented) The computer system of claim 45, wherein said optical path comprises a single optical path between said memory controller and at least one memory storage device for passing at least read/write data present on a plurality of electrical paths between said memory controller and at least one memory storage device.

74. (Previously Presented) The computer system of claim 45, wherein said optical path further passes command data between said memory controller and at least one memory storage device.

75. (Previously Presented) The computer system of claim 45, wherein said optical path further passes address data between said memory controller and at least one memory storage device.

76. (Previously Presented) The computer system of claim 45, wherein said single optical path further passes a clock signal between said memory controller and at least one memory storage device.

77. (Original) The computer system of claim 45, wherein said data includes read/write data which originates on a plurality of electrical paths, said optical path comprising a plurality of discrete optical guides respectively associated with said electrical path.

78. (Previously Presented) The computer system of claim 45, wherein said data includes command data which originates on a plurality of electrical paths, said optical path comprising a plurality of discrete optical guides respectively associated with said electrical path.

79. (Previously Presented) The computer system of claim 45, wherein said data includes address data which originates on a plurality of electrical paths, said optical path comprising a plurality of discrete optical guides respectively associated with said electrical path.

80. (Previously Presented) The computer system of claim 45, wherein said data includes clock signal data which originates on an electrical path, said optical path comprising a discrete optical guide respectively associated with said electrical path.

81. (Previously Presented) The computer system of claim 45, wherein said data includes clock signal data which originates on a plurality of electrical signal paths, said optical path comprising a plurality of discrete optical guides respectively associated with said electrical signal paths.

82. (Original) The computer system of claim 45, wherein said data includes control signal data which originates on an electrical signal path, said optical path comprising a discrete optical guide associated with said electrical signal path.

83. (Canceled)

84. (Previously Presented) The computer system of claim 45, wherein said processor, memory controller, at least one memory storage device and optical path are all integrated on the same die.

85-87. (Canceled)

88. (Previously Presented) The computer system of claim 68, wherein said memory module comprises an electro-optical converter for connecting optical data from said optical path to electrical signals for said at least one memory storage device.

89. (Previously Presented) An electro-optical converter for a memory system comprising:

at least one input arranged and configured to receive an electrical data signal from a memory controller;

at least one wavelength-adjustable device arranged and configured to convert said electrical data signal to an optical signal;

at least one optical output arranged and configured to transmit said optical signal into an optical path coupled directly to a memory module, said optical output, optical path and memory module being formed on a single die; and

a wavelength sensing mechanism connected to said controller arranged and configured to provide wavelength information to said controller with respect to the optical signal.

90. (Canceled)

91. (Original) The electro-optical converter of claim 89, wherein said optical output further comprises either a light emitting diode or injection laser diode.

92-94. (Canceled)

95. (Previously Presented) An electro-optical converter for a memory system comprising:

at least one input arranged and configured to receive an optical data signal from an optical path coupling said at least one input directly to a memory module;

at least one wavelength-adjustable electro-optical converter arranged and configured to convert said received data signal to an electrical signal;

at least one electrical output arranged and configured to transmit said electrical signal to an electrical path of a memory controller; and

a wavelength sensing mechanism arranged and configured to provide wavelength information to said controller with respect to an optical signal on said continuous optical path,

said input, optical path and memory module being formed on a single die.

96. (Canceled)

97. (Previously Presented) The electro-optical converter of claim 95, wherein said input further comprises a photodiode.

98. (Previously Presented) A memory system comprising:

a memory module having at least one input arranged and configured to receive an optical data signal from an optical path connecting directly between said at least one input and a memory controller;

at least one wavelength-adjustable electro-optical converter arranged and configured to convert said optical data signal received by said at least one input to an electrical signal; and

at least one electrical output arranged and configured to transmit said electrical signal to an electrical path of a memory storage device;

said input, optical path and memory controller being formed on a single die, and

said optical data signal comprising a plurality of multiplexed optical channels, wherein at least one channel is bidirectional and at least one channel is unidirectional.

99. (Canceled)

100. (Previously Presented) The memory system of claim 98, wherein said input further comprises a photodiode.

101. (Previously Presented) A method of operating a memory system comprising:

receiving an electrical signal output from a memory controller;

converting said electrical signal output from said controller to an optical signal for transmission on an optical path, said conversion step further comprising adjusting the wavelength of said optical path;

transmitting said optical signal over the optical path directly to a memory module; and

providing wavelength information to said controller with respect to the optical signal on said optical path,

said memory module, optical path and memory controller being formed on a single die.

102. (Previously Presented) The method of claim 101, further comprising:

said controller receiving data from said memory module through said optical path.

103. (Previously Presented) The method of claim 102, wherein said data includes at least one of read/write data.

104. (Previously Presented) The method of claim 102, wherein said data includes address data transmitted from said controller to said memory module.

105. (Previously Presented) The method of claim 102, wherein said data includes command data transmitted from said controller to said memory module.

106. (Original) The method of claim 102, wherein said data includes a clock signal.

107. (Original) The method of claim 102, wherein said data includes control data.

108. (Original) The method of claim 102, wherein said optical path comprises a plurality of multiplexed optical channels, said data being transmitted over said multiplexed optical channels.

109-110. (Canceled)

111. (Original) The method of claim 108, further comprising:

multiplexing said optical channels, and

demultiplexing said multiplexed optical channels.

112. (Original) The method of claim 108, further comprising:

multiplexing optical channels and providing multiplexed optical channels to said optical path; and

demultiplexing said multiplexed optical channels.

113. (Original) The method of claim 108, further comprising:

an optical multiplexer and demultiplexer located on each side of said optical path.

114. (Canceled)

115. (Previously Presented) The method of claim 101, further comprising:

an optical coupler at said memory module, having a connector for connecting with said optical path.

116. (Canceled)

117. (Previously Presented) The method of claim 117, wherein said controller provides wavelength adjustment information to said converter.

118. (Previously Presented) The method of claim 101, further comprising:

combining a plurality of electrical paths between said controller and memory module into a single optical path between said controller and memory module.

119. (Previously Presented) The method of claim 118 wherein said single optical path further passes command data between said controller and memory module.

120. (Previously Presented) The method of claim 118 further comprising:

passing address data between said controller and memory module along said single optical path.

121. (Canceled)

122. (Previously Presented) The method of claim 101, further comprising:

integrating a processor for communicating with said memory module with said controller, memory module, and optical path all within the same die.

123-125. (Canceled)

126. (Previously Presented) A method of operating a memory system comprising:

receiving an electrical signal output from at least one memory storage device;

converting said electrical signal output from said memory storage device to an optical signal for transmission on an optical path, said conversion step further comprising adjusting the wavelength of said optical signal;

transmitting said optical signal over an optical path to a memory controller controlling said at least one memory storage device; and

providing wavelength information to said controller with respect to the optical signal on said optical path,

said memory storage device, optical path and memory controller being formed on a single die.

127. (Previously Presented) The method of claim 126, further comprising:

said controller receiving data from said at least one memory storage device through said optical path.

128. (Previously Presented) The method of claim 127, wherein said data includes at least one of read/write data.

129. (Previously Presented) The method of claim 127, wherein said data includes address data transmitted from said controller to said at least one memory storage device.

130. (Previously Presented) The method of claim 127, wherein said data includes command data transmitted from said controller to said at least one memory storage device.

131. (Original) The method of claim 127, wherein said data includes a clock signal.

132. (Original) The method of claim 127, wherein said data includes control data.

133. (Original) The method of claim 127, wherein said optical path comprises a plurality of multiplexed optical channels, said data being transmitted over said multiplexed optical channels.

134-135. (Canceled)

136. (Original) The method of claim 133, further comprising:

multiplexing said optical channels, and

demultiplexing said multiplexed optical channels.

137. (Original) The method of claim 133, further comprising:

multiplexing optical channels and providing multiplexed optical channels to said optical path; and

demultiplexing said multiplexed optical channels.

138. (Original) The method of claim 133, further comprising:

an optical multiplexer and demultiplexer located on each side of said optical path.

139. (Previously Presented) The method of claim 126, wherein said at least one memory storage device is located on a memory module.

140. (Original) The method of claim 139, further comprising:

an optical coupler at said memory module, having a connector for connecting with said optical path.

141. (Canceled)

142. (Previously Presented) The method of claim 126, wherein said controller provides wavelength adjustment information to said converter.

143. (Previously Presented) The method of claim 126, further comprising:

combining a plurality of electrical paths between said controller and at least one memory storage device into a single optical path between said controller and at least one memory storage device.

144. (Previously Presented) The method of claim 143 wherein said single optical path further passes command data between said controller and at least one memory storage device.

145. (Previously Presented) The method of claim 143 further comprising:

passing address data between said controller and at least one memory storage device along said single optical path.

146. (Canceled)

147. (Previously Presented) The method of claim 126, further comprising:

integrating a processor for communicating with said at least one memory storage device with said controller, at least one memory storage device, and optical path all within the same die.

148-150. (Canceled)

151. (Original) The memory system of claim 9, wherein said plurality of multiplexed optical channels use Time Division Multiplexing (TDM).

152. (Original) The memory system of claim 9, wherein said plurality of multiplexed optical channels use Wave Division Multiplexing (WDM).

153. (Previously Presented) The memory system of claim 9, wherein said plurality of multiplexed optical channels use Frequency Division Multiplexing (FDM).

154. (Original) The memory system of claim 1, wherein said optical path optically passes compressed data.

155. (Original) The computer system of claim 53, wherein said plurality of multiplexed optical channels use Time Division Multiplexing (TDM).

156. (Original) The computer system of claim 53, wherein said plurality of multiplexed optical channels use Wave Division Multiplexing (WDM).

157. (Previously Presented) The computer system of claim 53, wherein said plurality of multiplexed optical channels use Frequency Division Multiplexing (FDM).

158. (Original) The computer system of claim 45, wherein said optical path optically passes compressed data.

159. (Original) The method of claim 108, wherein said plurality of multiplexed optical channels use Time Division Multiplexing (TDM).

160. (Original) The method of claim 108, wherein said plurality of multiplexed optical channels use Wave Division Multiplexing (WDM).

161. (Previously Presented) The method of claim 108, wherein said plurality of multiplexed optical channels use Frequency Division Multiplexing (FDM).

162. (Original) The method of claim 101, wherein said step of transmitting further comprises transmitting compressed data.

163. (Currently Amended) A memory system comprising:

a memory controller;

at least one memory module; and

a wavelength-adjustable device configured to provide an optical signal for communicating data between the memory controller and the at least one memory module, wherein:

the optical signal ~~comprises~~ is provided on multiplexed signal channels,

at least one signal channel is unidirectional, and

at least one signal channel is bidirectional.